UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/822,848	04/13/2004	Hajime Kimura	0756-7292	3205

31780 7590 06/18/2008

ERIC ROBINSON
PMB 955
21010 SOUTHBANK ST.
POTOMAC FALLS, VA 20165

EXAMINER	
XIAO, KE	

ART UNIT	PAPER NUMBER
2629	

MAIL DATE	DELIVERY MODE
06/18/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/822,848	KIMURA, HAJIME	
	Examiner	Art Unit	
	Ke Xiao	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 March 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-130* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-130* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-7, 32-49, 72-103 and 116-121 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shodo (US 6,404,137) in view of Resman (US 6,480,305).

Regarding **Claims 1-7 and 100-103**, Shodo teaches a semiconductor device (Shodo, Col. 2 lines 63-68) comprising:

a pixel portion comprising a plurality of pixels (Shodo, Fig. 2);

a first circuit (Shodo, Fig. 2, first shift register); and

a second circuit (Shodo, Fig. 2 element 9);

wherein each of the plurality of pixels comprises a sensor portion and a light emitting element portion (Shodo, Figs. 1-2 elements 1 and 2),

wherein the sensor portion comprises a first TFT, and the light emitting element portion comprises a second TFT (Shodo, Fig. 2 elements 41 and 42),

wherein the second circuit comprises a first logical circuit and a second logical circuit (Shodo, Fig. 2 element 9),

wherein the first TFT and the LED element is electrically connected to one of the first logical circuit and the second logical circuit, and the second TFT and the sensor element is electrically connected to the other (Shodo, Fig. 2, elements 9 and 41-42),

wherein the first circuit is configured to output a timing signal to the first logical circuit and to the second logical circuit (Shodo, Fig. 2 first shift register is configured to output timing to element 9),

wherein an image signal generated by the sensor portion is input to the light emitting element portion (Shodo, Fig. 2 element 32 feedback circuit to the light emitting element portion),

wherein one of the first logical circuit and the second logical circuit is configured to output a first signal to the first TFT, and the other is configured to output a second signal to the second TFT (Shodo, Fig. 2 elements 9 and 41-42),

wherein the first signal is different from the second signal (Shodo, Fig. 2 clearly the signals are different),

wherein the second circuit is so configured that, when one of the first logical circuit and the second logical circuit outputs an off signal to one of the first TFT and the second TFT, the other of the first logical circuit and the second logical circuit is outputs a pulse signal to the other of the first TFT and the second TFT (Shodo, Fig. 2, when the light emitting element is turned off there is an off signal applied to the gate of 41, additionally if the sensor is turned on there inherently needs to be a pulse signal applied to the gate of 42 in order to take the measurement of the intensity of the LED), and

wherein the second circuit is configured to select one of the sensor portion and the light emitting diode portion depending on a control signal, and output a pulse signal based on the timing signal to the one of the sensor portion and the light emitting element portion (Shodo, Figs. 1 and 2 elements 9, 41 and 42).

Shodo fails to teach a liquid crystal element portion as well as a backlight as claimed. Resman teaches that in the same field of endeavor a liquid crystal element with a backlight light emitting element can be used instead of just a light emitting element in the pixel portion (Resman, Fig. 2 and 3). It would have been obvious to one of ordinary skill in the art at the time of the invention to have utilized the liquid crystal element and backlight of Resman in the display device of Shodo in order to allow for the display device of Shodo to further operate as a scanner.

Regarding **Claims 32-37**, Shodo in view of Resman further teaches

wherein the first logical circuit is electrically connected to the first TFT through a first signal line (Shodo, Fig. 2 elements 9 and 41),

wherein the second logical circuit is electrically connected to the second TFT through a second signal line (Shodo, Fig. 2 elements 9 and 42), and

that the first signal line can be any one of a selection signal line, a reset signal line, and a liquid crystal selection signal line, and the second signal line can be any one of a sensor selection signal line and a sensor reset line (Shodo, Fig. 2 elements 7 and 8, 7 can operate as both selection as well as reset depending on the signal provided, and

8 can operates as both sensor select or sensor reset depending on the signal provided, Resman, Fig. 2 and 3).

Regarding **Claims 38-49**, Shodo further teaches that the first TFT can be any one of a selection TFT, a reset TFT, and a liquid crystal selection TFT, and the second TFT can be any one of a sensor selection, sensor reset TFT (Shodo, Fig. 2 elements 41 and 42, 41 can operate as both selection TFT as well as reset depending on the signal provided, and 42 can operates as both sensor select or sensor reset depending on the signal provided, and as mentioned in the previous rejection of Claims 1-7, the light emitting element section can easily be replaced with a liquid crystal element section).

Regarding **Claims 79-85, 116 and 117**, Shodo further teaches a display device using the above claimed semiconductor device (Shodo, Col. 1 lines 15-25).

Regarding **Claims 86-92, 118 and 119**, Resman further teaches that the semiconductor device can be also be used as a scanner (Resman Figs. 1 and 2).

Regarding **Claims 93-99, 120 and 121**, Shodo further teaches a portable information terminal using the above claimed semiconductor device (Shodo, Col. 1 lines 15-25, small self-illuminated device).

Regarding **Claims 72-78**, Shodo in view of Resman teaches that each pixel comprises one light emitting element and one photoelectric conversion element (Shodo, Figs. 1 and 2 LEDs and photo diodes). Shodo in view of Resman fails to teach that each pixel comprises three light emitting elements. The examiner takes official notice that it is well known in the art to use three light emitting elements in a single pixel for the

purposes of color reproduction, specifically red green and blue subpixels. It would have been obvious to one of ordinary skill in the art at the time of the invention to have three light emitting elements instead of one as taught by Shodo and Resman in order to easily produce a color image.

Regarding **Claims 122-130**, Shodo further teaches that the first circuit comprises shift register (Shodo, Fig. 2).

Claims 8-31, 50-61 and 104-115 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shodo (US 6,404,137) in view of Resman (US 6,480,305) as applied to Claims 1-7, 32-49, 79-103 and 116-121 in further view of Kubota (US 7,196,699).

Regarding **Claims 8-31, 104-111**, Shodo teaches a generic shift register with an output switching circuit (Shodo, Figs. 1 and 2). Shodo fails to teach that one of the first logical circuit and the second logical circuit is a NAND or AND circuit and the other is a NOR, or OR circuit. Kubota teaches the use of NAND, AND, NOR or OR gates as switching devices for outputs to the shift registers (Kubota, Fig. 75). It would have been obvious to one of ordinary skill in the art at the time of the invention to use the specialized shift register and switching section of Kubota instead of the generic shift registers of Shodo in order to reduce power consumption.

Regarding **Claims 50-61 and 112-115**, Shodo teaches a generic shift register with an output switching circuit (Shodo, Figs. 1 and 2). Shodo fails to teach that output

terminals of each of the first and second logical circuits is electrically connected to at least one inverter circuit. Kubota teaches a specialized shift register circuit with a switching section wherein the output terminals of all switching circuits are electrically connected to at least one inverter circuit (Kubota, Fig. 75). It would have been obvious to one of ordinary skill in the art at the time of the invention to use the specialized shift register and switching section of Kubota instead of the generic shift registers of Shodo in order to reduce power consumption.

Claims 62-64, are rejected under 35 U.S.C. 103(a) as being unpatentable over Shodo (US 6,404,137) in view of Resman (US 6,480,305) as applied to Claims 1-7, 32-49, 79-103 and 116-121 in further view of Chiyou (JP 11125841) and Nishigaki (US 6,246,180).

Regarding **Claims 62-64**, Shodo in view of Resman teaches a plurality of pixels comprising a light emitting element, a selection TFT, a driver TFT (Shodo, Fig. 2 elements 41 and driver TFT), and a photoelectric conversion element and a sensor selection TFT (Shodo, Fig. 2 element 42). Shodo in view of Resman fails to teach a sensor driver TFT and a sensor reset TFT.

Chiyou teaches a display scanner hybrid device with a photoelectric conversion element and a sensor TFT, a sensor driver TFT and a sensor reset TFT (Chiyou, Fig. 10 elements T1-T3 and 1001). It would have been obvious to use the pixel sensor circuitry

of Chiyou in the display scanner device of Shodo and Resman in order to increase the sensors sensitivity by adding the sensor driver TFT and the sensor reset TFT.

Shodo in view of Resman and Chiyou fails to teach a reset TFT as claimed. Nishigaki teaches a light emitting display device using a reset TFT (Nishigaki, Fig. 4 element 20). It would have been obvious to one of ordinary skill in the art at the time of the invention to use the reset TFT in conjunction with the display device of Shodo in view of Resman and Chiyou in order to provide improved image quality.

Claims 65-71, are rejected under 35 U.S.C. 103(a) as being unpatentable over Shodo (US 6,404,137) in view of Resman (US 6,480,305) as applied to Claims 1-7, 32-49, 79-103 and 116-121 in further view of Chiyou (JP 11125841).

Regarding **Claims 65-71**, Shodo in view of Resman teaches a plurality of pixels comprising a light emitting element, a selection TFT, a driver TFT (Shodo, Fig. 2 elements 41 and driver TFT), or a liquid crystal element, a liquid crystal selection TFT (Resman, Fig. 2 elements 124 and 128), and a photoelectric conversion element and a sensor selection TFT (Shodo, Fig. 2 element 42). Shodo in view of Resman fails to teach a sensor driver TFT and a sensor reset TFT.

Chiyou teaches a display scanner hybrid device with a photoelectric conversion element and a sensor TFT, a sensor driver TFT and a sensor reset TFT (Chiyou, Fig. 10 elements T1-T3 and 1001). It would have been obvious to use the pixel sensor circuitry

of Chiyou in the display scanner device of Shodo and Resman in order to increase the sensors sensitivity by adding the sensor driver TFT and the sensor reset TFT.

Response to Arguments

Applicant's arguments filed March 14th, 2008 have been fully considered but they are not persuasive.

Regarding independent Claims 1-7, 100 and 101, the applicant argues that Shodo fails to teach that the second circuit outputs a signal to the sensor portion. The examiner respectfully disagrees. Specifically, the claims are broad in their definition of "output to sensor portion". It can be interpreted as a signal that affects the sensor portion, which Shodo clearly teaches through the use of TFT 42 in figures 1 and 2.

Regarding the other outstanding rejections, the applicant makes no further arguments other than that they fail to cure the deficiencies addressed above.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ke Xiao whose telephone number is (571)272-7776. The examiner can normally be reached on Monday through Friday from 8:30AM to 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on (571) 272-3638. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Sumati Lefkowitz/
Supervisory Patent Examiner, Art Unit 2629

/Ke Xiao/
Examiner, Art Unit 2629